

***TLV320AIC12, TLV320AIC13  
TLV320AIC14, TLV320AIC15  
EVM***

*User's Guide*

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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## Preface

# Read This First

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### ***About This Manual***

This users guide describes the operation and use of the TLV320AIC12 codec family. A complete circuit description, schematic diagram, and bill of materials are also included.

### ***How to Use This Manual***

This document contains the following chapters:

- ☐ Chapter 1—EVM Overview
- ☐ Chapter 2—Digital Interface
- ☐ Chapter 3—Analog Interface
- ☐ Chapter 4—EVM Operation
- ☐ Chapter 5—TLV320AIC12/13/14/15 Bill of Materials
- ☐ Appendix A—TLV320AIC12/13/14/15 Schematic

### ***FCC Warning***

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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### **Data Sheets:**

TLV320AIC12  
TLV320AIC13  
TLV320AIC14  
TLV320AIC15

### **Literature Number:**

SLWS115B  
SLWS139A  
SLWS140A  
SLWS141A

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## EVM Overview

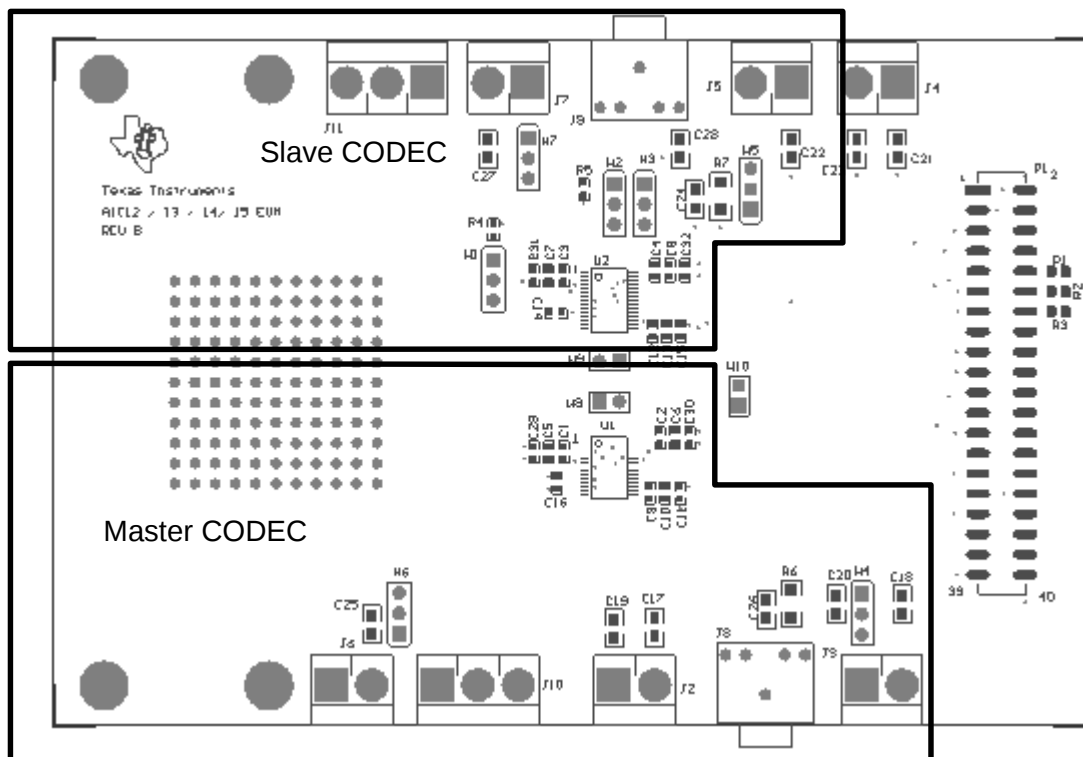
This user's guide supports the following devices:

- ☐ TLV320AIC12
- ☐ TLV320AIC13
- ☐ TLV320AIC14
- ☐ TLV320AIC15

This guide refers to the TLV320AIC12 only, since the remaining device feature sets are subsets of the TLV320AIC12. Any important differences are noted.

Figure 1–1. EVM

The EVM is split into two complementary halves as shown in Figure 1–1.



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# Digital Interface

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The digital signals required to operate this codec originate from the 40-pin connector—J1. There are two methods to drive the digital interface:

- ☐ Create a custom interface between the codec EVM and the host system.
- ☐ Alternatively, if a TI DSK (DSP starter kit) is the host system, a development platform is available from TI. This platform provides the additional functions that the codec requires in a convenient form factor.

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## 2.1 Codec-to-Platform

The TLV320AIC12, 13, 14, and 15 mate with the development platform via a 40-pin Samtec connector. The mating connector (Samtec part number, TSM-120-01-T-DV-P) is used on the development platform to provide the electrical connections necessary. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for more information.

The pinout for the 40-pin connector is listed in Table 2–1.

Table 2–1. Pinout for 40-Pin Connector

| Pin Number | Signal   | Description                      |
|------------|----------|----------------------------------|
| J21.1      | MCLK     | Master clock                     |
| J21.2      | DGND     | Digital ground                   |
| J21.3      | SCLK     | Serial data clock                |
| J21.4      | DGND     | Digital ground                   |
| J21.5      | DIN      | Data in                          |
| J21.6      | DGND     | Digital ground                   |
| J21.7      | DOUT     | Data out                         |
| J21.8      | Reserved | Reserved for future use          |
| J21.9      | FS       | Frame sync                       |
| J21.10     | Reserved | Reserved for future use          |
| J21.11     | CLKX     | Transmit clock                   |
| J21.12     | Reserved | Reserved for future use          |
| J21.13     | FSX      | Frame sync transmit              |
| J21.14     | Reserved | Reserved for future use          |
| J21.15     | DX       | Data transmit                    |
| J21.16     | DR       | Data receive                     |
| J21.17     | RESET    | Global reset for all devices     |
| J21.18     | FSR      | Frame sync receive               |
| J21.19     | PWDN     | Global powerdown for all devices |
| J21.20     | CLKR     | Receive clock                    |
| J21.21     | CNTLb    | GPIO pin                         |
| J21.22     | CNTLa    | GPIO pin                         |
| J21.23     | STATb    | Status pin                       |
| J21.24     | STATa    | Status pin                       |
| J21.25     | 3.3V_D   | Digital 3.3 V                    |
| J21.26     | Reserved | Reserved for future use          |
| J21.27     | 3.3V_D   | Digital 3.3 V                    |
| J21.28     | DGND     | Digital ground                   |
| J21.29     | 1.8V_D   | Digital 1.8 V                    |
| J21.30     | DGND     | Digital ground                   |
| J21.31     | 1.8V_D   | Digital 1.8 V                    |
| J21.32     | DGND     | Digital ground                   |

Table 2–1. Pinout for 40-Pin Connector (Continued)

| Pin Number | Signal     | Description                |
|------------|------------|----------------------------|
| J21.33     | 3.3V_A_DRV | Output driver supply 3.3 V |
| J21.34     | AGND       | Analog ground              |
| J21.35     | 3.3V_A_DRV | Output driver supply 3.3 V |
| J21.36     | AGND       | Analog ground              |
| J21.37     | 3.3V_A     | Analog 3.3 V               |
| J21.38     | AGND       | Analog ground              |
| J21.39     | 3.3V_A     | Analog 3.3 V               |
| J21.40     | AGND       | Analog ground              |

The development platform supports a number of functions that the codecs require. These are:

- ☐ MCLK generation
- ☐ Manual reset generation
- ☐ Power options

Refer to the *DSP – Codec Development Platform User's Guide* (SLAU090) for details regarding the development platform.

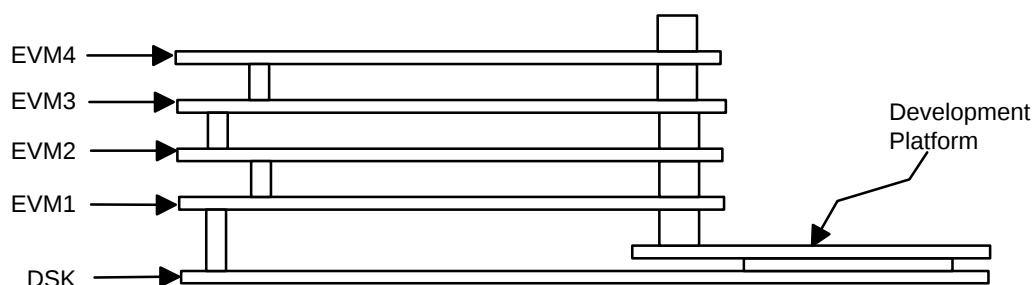
Further descriptions regarding the operation of this EVM assumes that the development platform is being used for all additional signals and power.

## 2.2 Codec-to-Codec

It is possible to cascade up to eight EVMs together. Since each EVM contains two codecs, this enables 16 codec channels to be chained together. The EVMs are cascaded simply by mating P1 of the board already resident to J1 of the next board via the 40-pin Samtec connector.

Figure 2–1 shows four EVMs connected together, giving a total of eight codecs in cascade. The master codec is always U1 on EVM1.

Figure 2–1. Cascade of Four EVMs



Note: Refer to SLAA141 for important information regarding the cascading of greater than four codecs.

EVM1 always defines the master codec in such a system.

## 2.3 Jumper Options

There are various jumpers on the board that can be configured in various ways, depending upon the user's requirements. Their functions are briefly presented in Table 2–2:

Table 2–2. Jumper Options

| Jumper      | Function                                                                                            |
|-------------|-----------------------------------------------------------------------------------------------------|
| W1          | Selects whether U2 is either a master or a slave codec                                              |
| W2          | Used along with W2 for correct polarity for FSD                                                     |
| W3          | Manages FSD from the master. Either connecting FSD to next co-dec or providing relevant polarity.   |
| W4          | Source for INM1b                                                                                    |
| W5          | Source for INM1a                                                                                    |
| W6          | Coupling for OUTP1b. Either directly or via capacitor.                                              |
| W7          | Coupling for OUTP1a. Either directly or via capacitor.                                              |
| W8          | Connects analog and digital ground together                                                         |
| W9          | Gives user the option of disconnecting the 3.3-V driver ground from the regular analog ground       |
| W10         | Use for odd number codec channels. Isolate the data from the co-dec not participating in the chain. |
| P1.9–P1.10  | Last FSD in the chain must be high                                                                  |
| P1.11–P1.12 | SCL must be high                                                                                    |
| P1.13–P1.14 | SDA must be high                                                                                    |

Since the EVM contains two codecs, there a variety of options available to the user:

- ☐ Stand-alone slave codec
- ☐ Single master codec
- ☐ Master/slave cascade

A fourth configuration exists when more than one EVM is required, this option is:

- ☐ Slave/slave

Each of these options are discussed in the following sections.

### 2.3.1 Stand-Alone Slave

This configuration applies to EVM1 only. When a single codec is to be used in slave mode, U2 is always the slave codec. Follow the jumper settings detailed in Table 2–3 for this condition.

Table 2–3. Stand-Alone Slave Jumper Settings

| Jumper      | 1–2          | 2–3          |
|-------------|--------------|--------------|
| W1          | Not inserted | Inserted     |
| W2          | Inserted     | Not inserted |
| W3          | Inserted     | Not inserted |
| W4          | Not inserted | Inserted     |
| P1.9–P1.10  | N/A          | N/A          |
| P1.11–P1.12 | Inserted     | Inserted     |
| P1.13–P1.14 | Inserted     | Inserted     |

### 2.3.2 Single Master Only

This configuration applies to EVM1 only. When a single codec is to be used in master mode, U2 is always the master codec. Follow the jumper settings detailed in Table 2–4 for this condition.

Table 2–4. Single Master Only Jumper Settings

| Jumper      | 1–2      | 2–3          |
|-------------|----------|--------------|
| W2          | Inserted | Not inserted |
| W3          | Inserted | Not inserted |
| W4          | Inserted | Not inserted |
| P1.9–P1.10  | N/A      | N/A          |
| P1.11–P1.12 | Inserted | Inserted     |
| P1.13–P1.14 | Inserted | Inserted     |

### 2.3.3 Master/Slave Cascade

This configuration applies to EVM1 only and is the factory-set shipping condition. When both codecs are used, both U1 and U2 are active. In this condition U2 is always the master codec, and U1 is always the slave codec. Follow the jumper settings detailed in Table 2–5.

Table 2–5. Master/Slave Cascade Jumper Settings

| Jumper      | 1–2          | 2–3          |
|-------------|--------------|--------------|
| W1          | Inserted     | Not inserted |
| W2          | N/A          | N/A          |
| W3          | Not inserted | Inserted     |
| W4          | Inserted     | Inserted     |
| P1.9–P1.10  | Inserted     | Inserted     |
| P1.11–P1.12 | Inserted     | Inserted     |
| P1.13–P1.14 | Inserted     | Inserted     |

### 2.3.4 Slave/Slave Cascade

This configuration applies to additional EVMs that may be installed for additional channels. It does not apply to EVM1. Both U1 and U2 are slave codecs to the master codec, which resides on EVM1. Follow the jumper settings detailed in Table 2–6.

*Table 2–6. Slave/Slave Cascade Jumper Settings*

| Jumper      | 1–2                                         | 2–3      |
|-------------|---------------------------------------------|----------|
| W1          | Not inserted                                | Inserted |
| W2          | N/A                                         | N/A      |
| W3          | Not inserted                                | Inserted |
| P1.9–P1.10  | Inserted only on the final EVM in the chain |          |
| P1.11–P1.12 | Inserted only on the final EVM in the chain |          |
| P1.13–P1.14 | Inserted only on the final EVM in the chain |          |

## 2.4 System Level Considerations

If the user chooses to cascade EVMs together, there are some system-level elements that should be understood with regard to jumper options.

### 2.4.1 Grounding Scheme

Each EVM allows the user to connect digital and analog grounds together. However, when more than one EVM is installed, remove this jumper from all EVMs but one, to minimize ground loops and maintain audio quality.

### 2.4.2 I<sup>2</sup>C Communications

I<sup>2</sup>C communications is achieved by the SCL and SDA signals. These signals are pulled high via jumpers inserted between P1.11–P1.12 and P1.13–P1.14. The jumpers should be removed to enable another EVM to be installed. Remember to install these jumpers on the last EVM in the chain.

### 2.4.3 FSD

The last EVM in the chain requires FSD be pulled high. This signal is pulled high via a jumper inserted between P1.9–P1.10. The jumper should be removed to enable another EVM to be installed. Remember to install this jumper on the last EVM in the chain.

## Analog Interface

Table 3–1 indicates the applicable connectors for each codec in the family. In order to enable a wide range of sources and loads to be connected to the codecs, screw terminals have been used wherever possible.

*Table 3–1. Analog Interface Connectors*

|                                | TLV320AIC12 |       | TLV320AIC13 |       | TLV320AIC14 |       | TLV320AIC15 |       |
|--------------------------------|-------------|-------|-------------|-------|-------------|-------|-------------|-------|
|                                | Master      | Slave | Master      | Slave | Master      | Slave | Master      | Slave |
| <b>Input Sources</b>           |             |       |             |       |             |       |             |       |
| Microphone input               | J9          | J8    | J9          | J8    | J9          | J8    | J9          | J8    |
| INP1                           | J5          | J3    | J5          | J3    | J5          | J3    | J5          | J3    |
| INP2                           | J4          | J2    | J4          | J2    | J4          | J2    | J4          | J2    |
| <b>Output Loads</b>            |             |       |             |       |             |       |             |       |
| OUTP1/OUTM1 600-Ω line output  | J7          | J6    | J7          | J6    | J7          | J6    | J7          | J6    |
| OUTP2/OUTP3 16-Ω driver output | J11         | J10   | J11         | J10   | NA          |       | NA          |       |



# EVM Operation

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The EVM is shipped from the factory in master/slave cascade mode. To check if the EVM is working properly, simply install the EVM onto the development platform, and apply power to the DSK. The EVM should begin working immediately.

In the default mode, the codecs recognize that there are two channels connected in the master/slave configuration, consequently the resultant SCLK and FS signals transmitted by the master codec adjust automatically based on the available MCLK.

It is now possible to calculate what should be observed after power up by calculating what FS and SCLK should be observed:

☐ FS

- In this example, MCLK is generated by the development platform and is equal to 100 MHz.
- $FS = MCLK / 16 \times m \times n \times p$
- Default values for m, n, and p are 16, 6, and 8 respectively
- $FS = 100 \times 10^6 / 16 \times 16 \times 6 \times 8$
- $FS = 8138 \text{ Hz}$

☐ SCLK

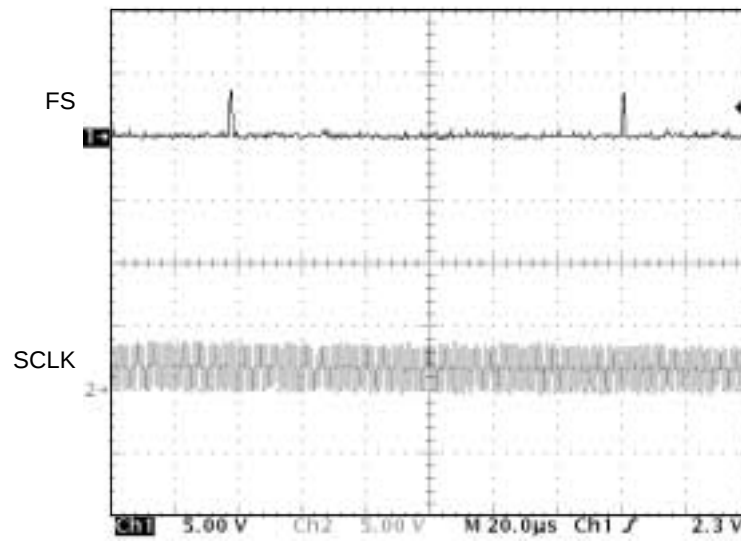
- $SCLK = 16 \times FS \times (\text{number of devices}) \times \text{mode}$
- $SCLK = 16 \times 8138 \times 2 \times 1$
- $SCLK = 260 \text{ kHz}$

FS can be observed either directly at the FS pin of U1 or U2 (pin 4) or on the development platform at TP9. SCLK can be observed easily at P1 pin 3 of the EVM or on the development platform at TP8.

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The captured signals are shown in Figure 4–1.

*Figure 4–1. EVM Captured Signals*



## TLV320AIC12/13/14/15 Bill of Materials

The following table contains a complete bill of materials for the TLV320AIC12/13/14/15 family of EVMs. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com) for questions regarding this EVM.

| Used | Value         | Ref Des                                                  | Description                                  | Vendor            | Part number         |
|------|---------------|----------------------------------------------------------|----------------------------------------------|-------------------|---------------------|
| 4    | 0.01 $\mu$ F  | C29 C30<br>C31 C32                                       | Capacitor 10000-pF 50-V ceramic Y5V 0603     | Panasonic         | ECJ-1VF1H103Z       |
| 12   | 0.1 $\mu$ F   | C5 C6 C7 C8<br>C9 C10 C11<br>C12 C13 C14<br>C15 C16      | Capacitor 0.1- $\mu$ F 25-V ceramic Y5V 0603 | Panasonic         | ECJ-1VF1E104Z       |
| 16   | 0.1 $\mu$ F   | C17 C18 C19<br>C20 C21 C22<br>C23 C24 C25<br>C26 C27 C28 | Capacitor 0.1- $\mu$ F 50-V ceramic X7R 0805 | Panasonic         | ECJ-2YB1H104K       |
| 4    | 1 $\mu$ F     | C1 C2 C3 C4                                              | Capacitor 1- $\mu$ F 10-V ceramic Y5V 0603   | Panasonic         | ECJ-1VF1A105Z       |
| 5    | 10 k $\Omega$ | R1 R2 R3 R4<br>R5                                        | Resistor 10-k $\Omega$ 1/16-W 5% 0603 SMD    | Panasonic         | ERJ-3GEYJ103V       |
| 2    | 10 k $\Omega$ | R6 R7                                                    | Resistor 10.0-k $\Omega$ 1/8-W 1% 1206 SMD   | Panasonic         | ERJ-8ENF1002V       |
| 2    |               | U1 U2 *                                                  | IC CODEC 1CH 16-bit 3.3-V 30 TSSOP           | Texas Instruments | TLV320AIC12IDBT     |
|      | * Alternate   |                                                          | IC SGL CH CODEC LP LV 30 TSSOP               | Texas Instruments | TLV320AIC13IDBT     |
|      | * Alternate   |                                                          | IC CODEC 1CH 16-bit 3.3-V 30 TSSOP           | Texas Instruments | TLV320AIC14IDBT     |
|      | * Alternate   |                                                          | IC SGL CH CODEC LP LV 30 TSSOP               | Texas Instruments | TLV320AIC15IDBT     |
| 1    |               |                                                          | TLV320AIC12 PWB                              | Texas Instruments | 6435621             |
| 1    |               | J1                                                       | 40-Pin SMT socket                            | Samtec            | SSW-120-22-F-D-VS-K |
| 1    |               | P1                                                       | 40-Pin SMT plug                              | Samtec            | TSM-120-01-T-DV-P   |
| 6    |               | J2 J3 J4<br>J5 J6 J7                                     | 2 Terminal screw connector                   | Lumberg           | KRMZ2               |
| 2    |               | J10 J11                                                  | 3 Terminal screw connector                   | Lumberg           | KRMZ3               |
| 2    |               | J8 J9                                                    | 161-3504                                     | Mouser            | 161-3504            |
| 3    |               | W8 W9 W10                                                | 2 Position jumper                            | Samtec            | TSW-102-07-L-S      |

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| Used | Value | Ref Des                    | Description                       | Vendor               | Part number       |
|------|-------|----------------------------|-----------------------------------|----------------------|-------------------|
| 7    |       | W1 W2 W3<br>W4 W5 W6<br>W7 | 3-Position jumper                 | Samtec               | TSW-103-07-L-S    |
| 2    |       | See Assy<br>Dwg            | 1.000/4-40 Nylon hex thread<br>SP | Keystone Electronics | 1902E             |
| 2    |       | See Assy<br>Dwg            | 0.500/4-40 Nylon hex thread<br>SP | Keystone Electronics | 1902C             |
| 2    |       | See Assy<br>Dwg            | 4-40 X 1/4 Machine screw PH<br>SS | Building Fasteners   | PMSSS 440 0025 PH |

## **TLV320AIC12/13/14/15 EVM Schematic**

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The TLV320AIC12/13/14/15EVM schematics are provided on the following pages.

|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|---|--|---|--|---|--|---|--|---|--|---|------------------|------------|--|----------|
| 1 |  | 2 |  | 3 |  | 4 |  | 5 |  | 6 |                  |            |  |          |
| D |  |   |  |   |  |   |  |   |  |   | Revision History |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   | REV              | ECN Number |  | Approved |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
| C |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
| B |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
| A |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
|   |  |   |  |   |  |   |  |   |  |   |                  |            |  |          |
| 1 |  | 2 |  | 3 |  | 4 |  | 5 |  | 6 |                  |            |  |          |

Analog\_IO

2xAIC12

Engineer: J.PURVIS

Drawn By: Y.DEWONCK

FILE: AIC12\_REVA

12500 TI Boulevard. Dallas, Texas 75243

Title: AIC12\_EVM

DOCUMENTCONTROL # 6435620

DATE: 5-Jul-2002

SIZE:

SHEET: 1 OF: 3

REV: B



